## WHAT IS CLAIMED IS:

1. A method for compensating for clock signal difference between a switch and a peripheral device, the switch comprising a first counter and a second counter, the switch being used for receiving and transmitting a plurality of packets, wherein each of the packets corresponds to a queue link node, an N-th packet corresponds to an N-th queue link node QLN(N) and an M-th packet corresponds to an M-th queue link node QLN(M), where N and M are integers, the method comprising:

a receiving process, the receiving process comprising the steps of:

- (a) receiving the N-th packet;
- (b) triggering the first counter;
- (c) performing a counting operation by the first counter;
- (d) proceeding to step (e) when an (N+1)-th packet is inputted to the switch, otherwise proceeding to said step (c);
- (e) stopping the first counter and then recording an inter-packet gap

  IPG(N, N+1) between the N-th packet and the (N+1)-th packet into the (N+1)-th queue

  link node QLN(N+1) according to a counting value by the first counter; and
  - (f) increasing N by one and then repeating from said step (b) to said step (f); and

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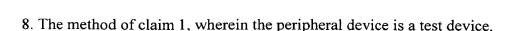
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a transmitting process, the transmitting process comprising the steps of:

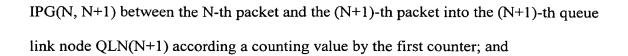
- (a1) reading the M-th queue link node QLN(M) corresponding to the M-th packet for obtaining an inter-packet gap IPG(M-1, M), and then transmitting the M-th packet;
  - (b1) triggering the second counter;
  - (c1) performing a counting operation by the second counter;
- (d1) stopping the counting operation of the second counter when a counted value by the second counter is equal to a clock cycle value corresponding to the inter-packet gap IPG(M-1, M), otherwise repeating said step (c1);
- (e1) reading an (M+1)-th queue link node QLN(M+1) corresponding to an (M+1)-th packet for obtaining an inter-packet gap IPG(M, M+1), and then transmitting the (M+1)-th packet; and
- (f1) increasing M by one and then repeating from said step (c1) to said step (f1).
- 2. The method of claim 1, wherein the switch further comprises a receive media access control (RMAC) unit for receiving the packets and a transmit media access control (TMAC) unit for transmitting the packets.
  - 3. The method of claim 2, wherein the first counter is in the RMAC unit and the second counter is in the TMAC unit.

- 4. The method of claim 1, wherein the N-th queue link node QLN(N) comprises:
- a first field for recording a memory address for temporally storing the (N+1)-th packet;
  - a second field for recording a destination port of the N-th packet;
- a third field for recording a size of the N-th packet; and a fourth field for recording an inter-packet gap IPG(N-1, N).
  - 5. The method of claim 4, wherein the N-th queue link node QLN(N) further comprises a fifth field for recording a source port speed of the N-th packet.
    - 6. The method of claim 1, wherein the N-th queue link node QLN(N) comprises:
  - a first field for recording a memory address for temporarily storing the (N+1)-th packet;
    - a second field for recording a destination port of the N-th packet;
    - a third field for recording a size of the N-th packet; and
- a fourth field for recording a clock cycle value corresponding to 96 bit time

  minus the inter-packet gap IPG(N-1, N).
  - 7. The method of claim 6, wherein the N-th queue link node QLN(N) further comprises a fifth field for recording a source port speed of the N-th packet.

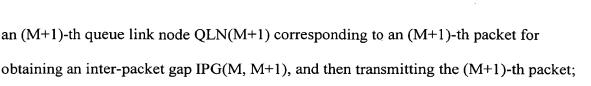


- 9. A method for compensating for clock signal difference between a switch and a peripheral device, the switch comprising a receive media access control (RMAC) unit for receiving a plurality of packets, a transmit media access control (TMAC) unit for receiving the packets, a first counter and a second counter, the switch being used for receiving and transmitting a plurality of packets, wherein each of the packets corresponds to a queue link node, an N-th packet corresponds to an N-th queue link node QLN(N), and an M-th packet corresponds to an M-th queue link node QLN(M), where N and M are integers, the method comprising:
  - a receiving process, the receiving process comprising the steps of:
- (a) proceeding to step (b) when the N-th packet is inputted to the switch, otherwise repeating said step (a);
- (b) proceeding to step (c) when the switch completely receives the N-th packet;
- (c) triggering the first counter;
  - (d) performing a counting operation by the first counter;
  - (e) proceeding to step (f) when an (N+1)-th packet is inputted to the switch, otherwise proceeding to said step (d);
    - (f) stopping the first counter and then recording an inter-packet gap

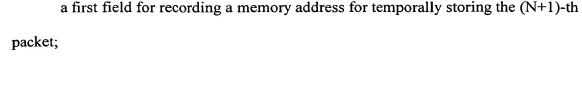


- (g) increasing N by one and then repeating from said step (b) to said step (g); and
- a transmitting process, the transmitting process comprising the steps of:
  - (a1) proceeding to step (b1) when an M-th packet in the switch waits to be transmitted;
  - (b1) reading the M-th queue link node QLN(M) corresponding to the M-th packet for obtaining an inter-packet gap IPG(M-1, M), and then transmitting the M-th packet;
    - (c1) triggering the second counter;
    - (d1) performing a counting operation by the second counter;
  - (e1) proceeding to step (f1) when a counted value by the second counter is equal to a clock cycle value corresponding to the inter-packet gap IPG(M-1, M), otherwise repeating said step (d1);
  - (f1) proceeding to step (g1) when an (M+1)-th packet in the switch waits for being transmitted, otherwise repeating said step (f1);
    - (g1) stopping the counting operation of the second counter and reading

and



- (h1) increasing M by one and then repeating from said step (c1) to saidstep (h1).
  - 10. The method of claim 9, wherein the first counter is in the RMAC unit and the second counter is in the TMAC unit.
  - 11. The method of claim 9, wherein the packets inputted to the switch are temporarily stored in a memory.
  - 12. The method of claim 9, wherein the N-th queue link node QLN(N) comprises:
  - a first field for recording a memory address for temporarily storing the (N+1)-th packet;
    - a second field for recording a destination port of the N-th packet;
- a third field for recording a size of the N-th packet; and
  - a fourth field for recording an inter-packet gap IPG(N-1, N).
  - 13. The method of claim 9, wherein the N-th queue link node QLN(N) comprises:



a second field for recording a destination port of the N-th packet;

a third field for recording a size of the N-th packet; and

a fourth field for recording a clock cycle value corresponding to 96 bit time minus the inter-packet gap IPG(N-1, N).

14. The method of claim 12 or 13, wherein the N-th queue link node QLN(N) further comprises a fifth field for recording a source port speed of the N-th packet.

15. The method of claim 9, wherein the peripheral device is a test device.

16. An apparatus for transceiving a plurality of packets, wherein each of the packets corresponds to a queue link node, an N-th packet corresponds to an N-th queue link node QLN(N), and an M-th packet corresponds to an M-th queue link node QLN(M), where N and M are integrals, the apparatus comprising:

a first counter and a second counter;

a receive media access control (RMAC) unit for receiving the packets, wherein the RMAC unit is used for triggering the first counter to obtain an inter-packet gap IPG(N, N+1) between the N-th packet and the (N+1)-th packet, and then recording the inter-packet gap IPG(N, N+1) into an (N+1)-th queue link node QLN(N+1); and

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a transmit media access control (TMAC) unit for transmitting the packets, wherein the TMAC unit is used for reading the M-th queue link node QLN(M) corresponding to the M-th packet for obtaining an inter-packet gap IPG(M-1, M), and then transmitting the M-th packet, and then triggering the second counter, wherein when a counted value by the second counter is equal to a clock cycle value corresponding to the inter-packet gap IPG(M-1, M), an (M+1)-th queue link node QLN(M+1)

17. The apparatus of claim 16, wherein the first counter is in the RMAC unit and the second counter is in the TMAC unit.

corresponding to an (M+1)-th packet is read for obtaining an inter-packet gap IPG(M,

M+1), and then the (M+1)-th packet is transmitted.

- 18. The method of claim 16, wherein the N-th queue link node QLN(N) comprises:
- a first field for recording a memory address for temporally storing the (N+1)-th packet;
- a second field for recording a destination port of the N-th packet;
  - a third field for recording a size of the N-th packet; and
  - a fourth field for recording the inter-packet gap IPG(N-1, N).
  - 19. The method of claim 16, wherein the N-th queue link node QLN(N) comprises:

a first field for recording a memory address for temporally storing the (N+1)-th packet;

a second field for recording a destination port of the N-th packet;

a third field for recording a size of the N-th packet; and

a fourth field for recording a clock cycle value corresponding to 96 bit time minus the inter-packet gap IPG(N-1, N).

20. The method of claim 18 or 19, wherein the N-th queue link node QLN(N)

further comprises a fifth field for recording a source port speed of the N-th packet.

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